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PATENT
Attorney Docket No. ASC-049C1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Fitzgerald		
SERIAL NO.:	10/774,890	GROUP NO.:	2818
FILING DATE:	February 9, 2004	EXAMINER:	Tran, Mai Huong
TITLE:	RELAXED SiGe PLATFORM FOR HIGH SPEED CMOS ELECTRONICS AND HIGH SPEED ANALOG CIRCUITS		

CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 1st day of October, 2004.

Wendy Martin

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is/are:

Transmittal Form (1 page); Supplemental Information Disclosure Statement (1 pg.); Form PTO-1449 (4 pgs.); Copies of cited references C102-C122; and Return Receipt Postcard

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TRANSMITTAL FORM

Application Serial Number	10/774,890
Filing Date	February 9, 2004
First Named Inventor	Fitzgerald
Group Art Unit	2818
Examiner Name	Tran, Mai Huong
Attorney Docket No.	ASC-049C1
Patent No.	Not applicable
Issue Date	Not applicable

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Check Attached
  - ☐ Copy of Fee Transmittal Form
- ☐ Amendment/Response
  - ☐ Preliminary
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
  - ☐ Letter to Official Draftsperson including Drawings [Total Sheets _____]
- ☐ Petition for Extension of Time
- ☒ Supplemental Information Disclosure Statement
  - ☒ Form PTO-1449
  - ☒ Copies of IDS Citations C102-C22
- ☐ Certified Copy of Priority Document(s)
- ☐ Sequence Listing submission
  - ☐ Paper Copy/CD
  - ☐ Computer Readable Copy
  - ☐ Statement verifying identity of above
- ☐ Copy of Notice to File Missing Parts of Application
- ☐ Formal Drawing(s)
- ☐ Request For Continued Examination (RCE) Transmittal
- ☐ Power of Attorney (Revocation of Prior Powers)
- ☐ Terminal Disclaimer
- ☐ Executed Declaration and Power of Attorney for Utility or Design Patent Application
- ☐ Small Entity Statement
- ☐ CD(s) for large table or computer program
- ☐ Amendment After Allowance
- ☐ Request for Certificate of Correction
  - ☐ Certificate of Correction (in duplicate)
- ☐ Notice of Appeal to Board of Patent Appeals and Interferences
- ☐ Appeal Brief (in triplicate)
- ☐ Status Inquiry
- ☒ Return Receipt Postcard
- ☒ Certificate of First Class Mailing under 37 C.F.R. 1.8
- ☐ Certificate of Facsimile Transmission under 37 C.F.R. 1.8
- ☐ Additional Enclosure(s) *(please identify below)*

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Respectfully submitted,

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Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

The references listed on the enclosed PTO-1449 are submitted solely in compliance with the duty of candor. It is understood that this Information Disclosure Statement does not fall within the provisions of 37 C.F.R. §1.97. In accordance with the U.S. Patent Office's partial waiver of the requirement under 37 C.F.R. 1.98(a)(2)(i), only copies of the non-patent publications are enclosed.

It is respectfully requested that the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

Respectfully submitted,

Date: Oct. 1, 2004
Reg. No. 44,381

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FORM PTO – 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-049C1 APPLICANT(S): Fitzgerald SERIAL NO.: 10/774,890 FILING DATE: February 9, 2004 GROUP: 2818

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A170	2002/0063292	05/30/2002	Armstrong *et al.*			
	A171	2002/0190284	12/19/2002	Murthy *et al.*			12/30/1999
	A172	2004/0007724	01/15/2004	Murthy *et al.*			07/12/2002
	A173	2004/0014276	01/22/2004	Murthy *et al.*			07/16/2002
	A174	2004/0070035	04/15/2004	Murthy *et al.*			07/23/2003
	A175	2004/0084735	05/06/2004	Murthy *et al.*			07/23/2003
	A176	2004/0119101	06/24/2004	Schrom *et al.*			12/23/2002
	A177	2004/0142545	07/22/2004	Ngo *et al.*			01/17/2003
	A178	2004/0173815	09/09/2004	Yeo *et al.*			03/04/2003
	A179	5,089,872	02/18/1992	Ozturk *et al.*			
	A180	5,242,847	09/07/1993	Ozturk *et al.*			
	A181	6,228,694	05/08/2001	Doyle *et al.*			
	A182	6,235,568	05/22/2001	Murthy *et al.*			
	A183	6,281,532	08/28/2001	Doyle *et al.*			
	A184	6,326,664	12/04/2001	Chau *et al.*			
	A185	6,563,152	05/13/2003	Roberds *et al.*			12/29/2000
	A186	6,605,498	08/12/2003	Murthy *et al.*			03/29/2002
	A187	6,621,131	09/16/2003	Murthy *et al.*			11/01/2001
	A188	6,657,223	12/02/2003	Wang *et al.*			10/29/2002
	A189	6,703,648	03/09/2004	Xiang *et al.*			10/29/2002
	A190	6,743,684	06/01/2004	Liu			10/11/2002

EXAMINER	DATE CONSIDERED

FORM PTO – 1449 SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTORNEY DOCKET NO.: ASC-013 APPLICANT(S): Bulsara *et al.* SERIAL NO.: 10/218,007 FILING DATE: August 13, 2002 GROUP: 2813

U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)

OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C102	Gannavaram, *et al.*, "Low Temperature (≤800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS," IEEE International Electron Device Meeting Technical Digest, (2000), pp. 137-440.
	C103	Ge *et al.*, "Process-Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering," IEEE International Electron Devices Meeting Technical Digest, (2003) pp. 73-76.
	C104	Ghani *et al.*, "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," IEEE International Electron Devices Meeting Technical Digest, (2003), 11.6.1-11.6.3.
	C105	Hamada *et al.*, "A New Aspect of Mechanical Stress Effects in Scaled MOS Devices," IEEE Transactions on Electron Devices, Vol. 38, No. 4 (April 1991), pp. 895-900.
	C106	Huang *et al.*, "Isolation Process Dependence of Channel Mobility in Thin-Film SOI Devices," IEEE Electron Device Letters, Vol. 17, No. 6 (June 1996), pp. 291-293.
	C107	Huang *et al.*, "LOCOS-Induced Stress Effects on Thin-Film SOI Devices," IEEE Transactions on Electron Devices, Vol. 44, No. 4 (April 1997), pp. 646-650.
	C108	Huang, *et al.*, "Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $Si_{1-x}Ge_x$ Source/Drain", IEEE Electron Device Letters, Vol. 21, No. 9, (Sept. 2000) pp. 448-450.
	C109	Iida *et al.*, "Thermal behavior of residual strain in silicon-on-insulator bonded wafer and effects on electron mobility," Solid-State Electronics, Vol. 43 (1999), pp. 1117-1120.

EXAMINER	DATE CONSIDERED

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OTHER ART, JOURNAL ARTICLES, ETC.

EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C110	Ito *et al.*, "Mechanical Stress Effect on Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design," IEEE International Electron Devices Meeting Technical Digest, (2000), pp. 247-250.
	C111	Lochtefeld *et al.*, "Investigating the Relationship Between Electron Mobility and Velocity in Deeply Scaled NMOS via Mechanical Stress," IEEE Electron Device Letters, Vol. 22, No. 12 (2001), pp. 591-593.
	C112	Ootsuka *et al.*, "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Applications," IEEE International Electron Devices Meeting Technical Digest, (2000), pp. 575-578.
	C113	Ota *et al.*, "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," IEEE International Electron Devices Meeting Technical Digest, (2002), pp. 27-30.
	C114	Öztürk, *et al.*, "Advanced $Si_{1-x}Ge_x$ Source/Drain and Contact Technologies for Sub-70 nm CMOS," IEEE International Electron Device Meeting Technical Digest, (2002), pp. 375-378.
	C115	Öztürk, *et al.*, "Ultra-Shallow Source/Drain Junctions for Nanoscale CMOS Using Selective Silicon-Germanium Technology," Extended Abstracts of International Workshop on Junction Technology, (2001), pp. 77-82.
	C116	Öztürk, *et al.*, "Selective Silicon-Gremanium Source/Drain Technology for Nanoscale CMOS," Mat. Res. Soc. Symp. Proc., Vol. 717, (2002), pp. C4.1.1-C4.1.12.
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	C118	Shimizu *et al.*, "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," IEEE International Electron Devices Meeting Technical Digest, (2001), pp. 433-436.

EXAMINER	DATE CONSIDERED

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EXAM. INIT.		OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)
	C119	Thompson *et al.*, "A Logic Nanotechnology Featuring Strained-Silicon," IEEE Electron Device Letters, Vol. 25, No. 4 (April 2004), pp. 191-193.
	C120	Thompson *et al.*, "A 90 nm Logic Technology Featuring 50nm Strained-Silicon Channel Transistors, 7 layers of Cu *Interconnects*, Low k ILD, and 1um^2 SRAM Cell," IEEE International Electron Devices Meeting Technical Digest, (2002), pp. 61-64.
	C121	Tiwari *et al.*, "Hole Mobility Improvement in Silicon-on-Insulator and Bulk Silicon Transistors Using Local Strain," IEEE International Electron Devices Meeting Technical Digest, (1997), pp. 939-941.
	C122	Uchino, *et al.*, "A Raised Source/Drain Technology Using In-situ P-doped SiGe and B-doped Si for 0.1-μm CMOS ULSIs," IEEE International Electron Device Meeting Technical Digest, (1997), pp. 479-482.

EXAMINER	DATE CONSIDERED

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